REMARKS

The final Office Action of May 22, 2006, has been received and reviewed.

Claims 1, 3, 5-25, 28-35, and 53-54 are currently pending in the above-referenced application. Of these, claims 9, 24, and 29 have been withdrawn from consideration. Claims 1, 3-23, 25, 28, 30-35, 53, and 54, which have been considered, stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 18-21, 30, 31, 33-35 and 54 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in U.S. Patent 6,437,449 to Foster (hereinafter "Foster").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claim 18 is directed to a semiconductor device assembly that includes a substrate, a first semiconductor device, a second semiconductor device, and spacers between the first and second semiconductor devices. The spacers, which protrude from a surface of the first semiconductor device, are "mutually laterally spaced" and "discrete" from one another. They communicate with a ground or reference voltage plane of the first semiconductor device, and with a back side of the second semiconductor device.

Foster describes a packaged multi-chip module assembly. A semiconductor die 108 is mounted to and is in communication with a die-mounting pad 104 that is part of substrate 102. Col. 2, lines 63-64; col. 3, lines 7-12; FIG. 2. A single, planar spacer 116 is mounted to, and in electrical isolation from, the front surface 110 of the first semiconductor die 108. Col. 3, lines 20-21, 45-46; FIG. 2.

It is respectfully submitted that Foster does not expressly or inherently describe each and every element of independent claim 18. Specifically, it is evident that Foster lacks any express or

inherent description of "mutually laterally spaced discrete spacers positioned on and protruding from an active surface of [a] first semiconductor device." To repeat: each assembly described in Foster includes only one planar spacer 116. Therefore, Foster does not anticipate each and every limitation of independent claim 18, as would be required to maintain the 35 U.S.C. §102(e) rejection of independent claim 18.

Each of claims 19-21, 30, 31, 33-35, and 54 is allowable among other reasons, for depending directly or indirectly from independent claim 18, which is allowable.

Claim 33 is further allowable because Foster includes no express or inherent description of a semiconductor device assembly that includes three or more semiconductor devices.

Claim 54 is additionally allowable since Foster neither expressly nor inherently describes a semiconductor device assembly with at least one spacer that is secured to a contact pad of a semiconductor device. To the contrary, Foster explains that the spacer 116, 216 of a semiconductor device assembly may not be positioned over a bond pad 112 of a semiconductor device 108. Col. 3, lines 38-51. Instead, the spacers 116 and 216 are configured to have an outer periphery which is smaller than the inner periphery of a bond pad 112 arrangement of the semiconductor device 108 so that the spacers 116 and 216 may be located within the inner periphery of the bond pads 112 and, thus, do not cover the bond pads 112. *Id.*

Withdrawal of the 35 U.S.C. § 102(e) rejections of claims 18-21, 30, 31, 33-35, and 54 is respectfully requested, as is the allowance of each of these claims.

Rejections under 35 U.S.C. § 103(a)

Claims 1, 3, 5-8, 10--23, 25, 28, 30-35, 53, and 54 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference

> or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Pu in View of LoBianco

Claims 1, 3, 5-8, 10, 12-17, and 53 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over that taught in U.S. Patent 6,593,662 to Pu et al. (hereinafter "Pu"), in view of teachings from U.S. Patent 6,340,846 to LoBianco et al. (hereinafter "LoBianco").

In maintaining this rejection, the Examiner has cited numerous court opinions regarding when a reference does or does not teach away from the combination of its teachings with teachings of other art or from claimed subject matter. Notably, in each of the opinions that has been cited by the Examiner, the feature from which each reference purportedly "taught away" was actually within the scope of the disclosed subject matter. In contrast, the teachings or Pu are quite clearly limited to structures and assemblies that reduce the so-called "cushion effect," an effect that is realized during wirebonding and similar processes, that occurs when compressible materials, such as polyimide tape, are used to secure semiconductor devices in stacked relation to one another. *See, e.g.,* col. 2, lines 12-14; col. 2, lines 21-23; col. 3, lines 15-19; col. 4, lines 35-39.

The teachings of Pu relate to, and are limited to, stacked multi-chip structures in which rigid adhesive materials are employed. *See, e.g.,* col. 3, lines 15-19; col. 4, lines 35-39. In such a structure, a rigid adhesive layer 204a adheres a first die 206 to a substrate 202. Col. 4, lines 13-15; FIGs. 4A, 4B. The rigid adhesive layer 204b adheres spacers 220 to the first die 206, and a second rigid adhesive layer 204c adheres a second die 208 to the tops of the spacers 220. Col. 4, lines 17-20; FIGs. 4A, 4B. Pu teaches that the spacers 220 may be formed from silicon or metal (col. 4, lines 47-53), both of which provide sufficient rigidity to avoid compression.

LoBianco teaches a stacked multi-chip package. A first die 14 is secured to the top surface of a substrate 12 with an adhesive layer 13. Col. 3, lines 50-55; FIG. 3. Conductive wires 38 electrically connect bond pads of the die 14 and corresponding terminals of the substrate 12. A spacer 50 may be placed atop and secured to the first die 14 with a layer of adhesive 54. Col. 6, lines 60-68; FIG. 8. Another adhesive layer 40 is then dispensed onto the top of the first die 14 and around the spacer 50. That adhesive layer 40, as well as an adhesive layer 52 that has been applied to the spacer 50, secure a second die 16 over the spacer 50 and the first die 14. Col. 6, line 66, to col. 7, line 4; FIG. 8.

The Examiner has asserted that resiliently compressible materials – specifically, polyimide – may be used to form the spacer 50 of the assembly taught in LoBianco. *See, e.g.,* Office Action of November 23, 2005, pages 2-4.

It is respectfully submitted that there are several reasons that the teachings of Pu and LoBianco do not support a *prima facie* case of obviousness against any of claims 1, 3, 5-8, 10, 12-17, or 53.

First, it is respectfully submitted that Pu teaches away from the asserted combination of reference teachings. It has been asserted that one of ordinary skill in the art would have been motivated to replace the silicon or metal spacer 116 of Pu with a polyimide spacer 50 of LoBianco. Office Action of November 23, 2005, pages 2-4. It has been further asserted that a polyimide spacer 50 of the type taught in LoBianco would inherently be resiliently compressible. Office Action of November 23, 2005, page 4. It is respectfully submitted that these assertions overlooks that fact that the teachings of Pu are limited to semiconductor device assemblies that are configured to minimize the so-called "cushion effect," and that the use of a resiliently compressible spacer would not minimize but, rather, increase the "cushion effect." In fact, Pu specifically teaches that "polyimide . . . causes the cushion effect . . ." Col. 2, lines 12-14.

Second, it is respectfully submitted that Pu teaches away from the subject matter recited in independent claim 1. Specifically, with respect to independent claim 1, a semiconductor device assembly that includes "at least one resiliently compressible spacer" that protrudes from a

surface of one semiconductor device and defines a distance between that semiconductor device and another semiconductor device.

Third, it is respectfully submitted that, in view of the fact that Pu teaches away from the combination of its teachings with the teachings of LoBianco, as well as from the subject matter to which independent claim 1 is directed, that one of ordinary skill in the art wouldn't have been motivated to combine teachings from Pu and LoBianco in the manner that has been asserted. Rather, it appears that the rejection of claims 1, 3, 5-8, 10, 12-17, and 53 is based solely and impermissibly upon the hindsight provided by the subject matter recited in these claims.

As a *prima facie* case of obviousness has not been established against any of claims 1, 3, 5-8, 10, 12-17, or 53, it is respectfully submitted that the subject matter to which each of these claims is directed is allowable under 35 U.S.C. § 103(a).

Claim 8 is additionally allowable because neither Pu nor LoBianco teaches or suggests a semiconductor device assembly that includes an adhesive material located between adjacent spacers.

Claim 17 is further allowable since Pu and LoBianco both lack any teaching or suggestion of a semiconductor device assembly that includes at least one resiliently compressible spacer secured to a noncircuit bond pad of a semiconductor device.

Claim 53 is also allowable since neither Pu nor LoBianco teaches or suggests a semiconductor device assembly that includes at least one resiliently compressible spacer secured to a contact pad of a semiconductor device.

Pu, LoBianco, and Foster

Claims 11, 22, 18-23, 25, 28, 30-35, and 54 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Pu, in view of teachings from LoBianco and, further, in view of the subject matter taught in Foster.

Claims 11 and 12 are both allowable, among other reasons, for depending indirectly and directly, respectively, from independent claim 1, which is allowable.

Furthermore, it is respectfully submitted that Foster, which teaches assemblies that includes spacers 116 that may be formed from rigid materials, such as copper, silicon, Alloy 42, a

ceramic, silicon dioxide, or a composite material (col. 3, lines 22-33), does not provide any teaching or suggestion that counters the facts that Pu teaches away from the combination of its teachings with those of LoBianco, that Pu teaches away from the subject matter recited in claims 11, 22, 18-23, 25, 28, 30-35, and 54, and that one of ordinary skill in the art ordinary skill wouldn't have been motivated to combine the teachings of Pu with those of LoBianco in the manner that has been asserted.

Therefore, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 11, 12, 18-23, 25, 30-35, or 54, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

Foster in View of LoBianco

Claims 1, 3, 5-8, and 10-16 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Foster, in view of the subject matter taught in LoBianco.

As discussed above, neither LoBianco nor Foster teaches or suggests a semiconductor device assembly that includes a resiliently compressible spacer, as would be required for the combined teachings of LoBianco and Foster to teach or suggest each and every element of independent claim 1. As such, it is respectfully submitted that, without the benefit of hindsight that the rejected claims provide to the Examiner, one or ordinary skill in the art wouldn't have been motived to combine the teachings of Foster and LoBianco in the manner that has been asserted or had any reason to expect that the purported combination of reference teachings would have been successful. Therefore, LoBianco and Foster do not meet any of the criteria set forth in M.P.E.P. § 706.02(j) that would be necessary to establish a *prima facie* case of obviousness against claims 1, 3, 5-8, and 10-16.

It is respectfully that the 35 U.S.C. § 103(a) rejections of claims 1, 3, 5-8, 10--23, 25, 28, 30-35, 53, and 54 be withdrawn, and that each of these claims be allowed.

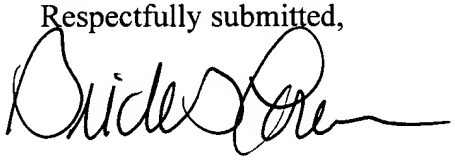
Election of Species Requirement

It is respectfully submitted that independent claim 1 remains generic to both of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of this claim, claims 9, 24, and 29, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1, 3, 5-25, 28-35, 53 and 54 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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